4th International Energy Conversion Engineering Conference and Exhibit (IECEC)
26 - 29 June 2006, San Diego, California

AIAA 2006-4022

NEPTUNE Power System: Science Node Converter Startup Operations Design and Implementation Circuit

Shuai Lu[*] and Mohamed A. El-Sharkawi[†]
Electrical Engineering Department, University of Washington, Seattle, WA, 98105

Harold Kirkham[‡] and Vatche Vorperian[§]
Jet Propulsion Laboratory, California Institute of Technology, CA, 91109

Bruce M. Howe[**]
Applied Physics Laboratory, University of Washington, Seattle, WA, 98105

***Abstract* – The North-East Pacific Time-series Undersea Networked Experiments (NEPTUNE) is an underwater power and communications network for scientific experiments. It is proposed for the ocean floor of the Juan de Fuca tectonic plate in the Northeast Pacific Ocean. The NEPTUNE power system is a 10 kV dc network. In the science nodes connected to the NEPTUNE network, 10 kV to 400 V dc-dc converters are used to power various scientific instruments and underwater vehicles. The focus of this paper is the startup circuit design and its implementation. The configuration of the NEPTUNE power system is introduced and the challenges of the system resulting from its location on the seafloor are addressed. A set of operations designed to start the 10 kV converters, which includes the control of the 10 kV switches connecting input power cables to converters, checking converter internal faults, and the starting of these converters, is described using a logic sequence diagram. The concept is tested and results are provided.**

I. Introduction

Oceans occupy 70 percent of the earth's surface and greatly affect global climate, biological diversity, geological activities, and many other global eco-system processes. To understand the complexity and interactive dynamics of ocean systems, data should be collected on many temporal and spatial scales. This poses a great challenge, as scientists must build long-term ocean observatories to enable the acquisition of sustained time series data sets. The need for long-term data acquisition requires continuous power and communications, which is the main focus of the North-East Pacific Time-series Undersea Networked Experiments (NEPTUNE).

NEPTUNE is a planned cabled network consisting of 3,000 km of fiber-optic/power cable on the seafloor encircling the Juan de Fuca tectonic plate beneath the Northeast Pacific Ocean to provide power and communications to a multitude of undersea observatories [1, 2]. These observatories will allow us the exploration of many oceanographic and geophysical systems in a long-term and real-time approach, which is difficult to carry out using present techniques [3-5].

The NEPTUNE system has two main subsystems: power and communications. This paper addresses one important aspect of the NEPTUNE power system.

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[*] PhD student, University of Washington, Department of EE, Paul Allen Center Room AE100R, Campus box 352500, Seattle, WA.
[†] Professor, University of Washington, Department of EE, Paul Allen Center Room AE100R, Campus box 352500, Seattle, WA.
[‡] Principal, Reliability Technology Group, Jet Propulsion Laboratory, California Institute of Technology, Pasadena, CA.
[§] Senior Engineer, Power and Sensor Electronics Group, Jet Propulsion Laboratory, California Institute of Technology, Pasadena, CA.
[**] Principal Oceanographer, Applied Physics Laboratory, University of Washington, Seattle, WA.

The topology of the NEPTUNE system is shown in Fig. 1. The NEPTUNE power system is a network of dc cables energized by two shore stations: one on Vancouver Island in Canada, and the other on the Oregon coast of the USA. The red dots represent branching unit (BU) locations, where different cable sections are connected. Scientific instruments are connected to the network through science nodes, using spur cables coming from the BU's, as shown in the layout in Fig. 2. The backbone and spur cables are standard marine communication cables with both power delivery and fiber optic communication capabilities [6].

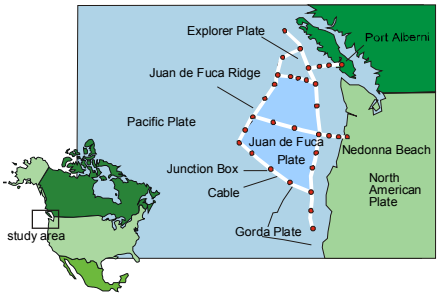

Figure 1. NEPTUNE cable system

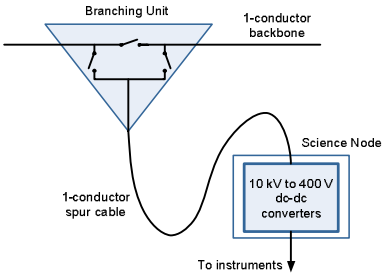

Figure 2. Layout of science node connection

The NEPTUNE power system is different from the terrestrial counterpart in many ways. In the science nodes, for example, 1) The underwater hardware is difficult to access, therefore every component in the system must be very reliable and maintenance free. (A system-wide goal of no more than four ship visits per year to repair the power systems of 30 science nodes was adopted by the NEPTUNE power group.) 2) No low voltage auxiliary supply is readily available (battery usage is excluded for long-term reliability reason) to power the switching operations and logic functions during system startup and 3) No communications exist before the power system is fully operational. Because there is no power and no communications, the startup of the power system must be autonomous.

New methods need to be developed to meet these challenges imposed on the design of hardware, operations and controls of NEPTUNE power system. The reliability issue has to be borne in mind throughout the design process. The lack of battery power issue is addressed in [7], which developed a 12 V startup power supply from 10 kV input. This paper focuses on the operations designed for starting up the science node power system and its implementation circuit, aiming at solving the autonomy issue.

II. Science Node Converter Startup Operations

A. Science node configuration

A block diagram of the science node power system configuration is shown in Fig. 3.

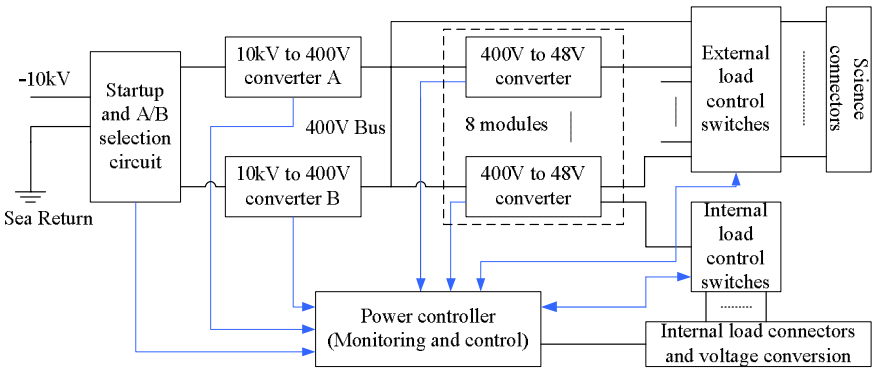

Figure 3. Science node power system block diagram

A voltage level of -10 kV was selected for the backbone of NEPTUNE power system [6]. Using negative voltage supply avoids the corrosion of the electrodes at the science nodes. The 10 kV to 400 V dc-dc converters in the science nodes accept input voltages ranging from -5.5 kV to -10 kV. Outside this range, the converter is disabled.

The output of the converter is up to 10 kW at 400 V [1]. In each science node, there are two 10 kV dc-dc converters, with one in cold standby. The converters are connected to the spur cable through high voltage latching switches as shown in Fig. 4.

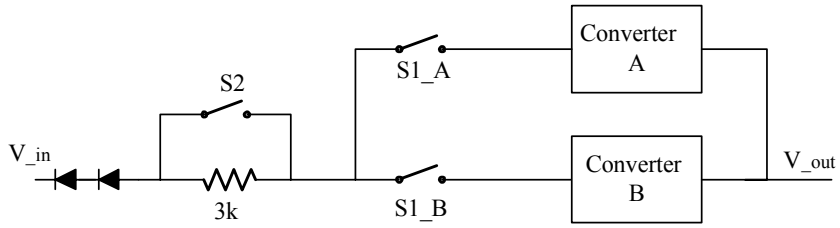

Figure 4. Science node converters input circuit configuration

The initial startup of the science node is controlled locally by a startup and A/B selection circuit. After one of the two converters starts, 400 V and 48 V are available for science loads and internal loads such as power controllers and the communications subsystem. Then, the shore stations are able to take control of the system operations remotely.

B. Startup operations of science node power system

The function of high voltage latching switches S1_A and S1_B in Fig. 4 is to power the converters or isolate them from the input high voltage power cable. It is desired that a converter is disconnected from V_in when it is not operating, so that less voltage stress will be imposed on the components. The 3 kΩ resistor is to limit the initial charging current into the capacitance of the converters input filter, when S1_A or S1_B is closed. It is bypassed by S2 afterwards. The switches S1_A, S1_B and S2 are vacuum type latching switches. To extend their lifetime, the control for the switches is designed to operate them only at low current.

The science node power system has to be autonomous during startup since the communications system is not yet operational. The challenge is how to inform the seafloor science nodes of the intended operation. Some sort of signal must be sent from the shore stations. This is achieved by using different voltage levels and polarities at the shore stations as communication signals. The startup sequence of operations is performed, in conjunction with the shore stations, in 11 steps:

1) All switches in Fig. 4 are latched open when the shore station voltage is set to a positive voltage of about 500 V; the positive voltage is the signal for only this action.

2) After a few minutes, the shore station voltage is reversed to about -500 V. This low value of negative voltage is the signal for switch S1_A (only) to be closed;

3) Fault condition is checked at the input of converter A. If a fault exists, a non-zero current will flow, and switch S1_A is opened;

4) Whether or not a fault is detected, switch S1_B is closed;

5) Fault condition is checked at the input of converter B. If a fault exists, switch S1_B is opened;

6) The shore station voltage is increased to -10 kV gradually.

7) Switch S2 is closed when the voltage reaches -5.5 kV so that the resistor is bypassed before the converter starts.

8) The control circuit for converter A is powered

9) If the output voltage rises to 400 V, switch S1_B is opened;

10) If converter A cannot start, converter B is turned on and switch S1_A is opened;

11) If converter B cannot start, switch S1_B is opened.

Step 1 is to reset the science node power system to a fixed and known pre-start condition. Positive polarity of the operating voltage is used in this step to reduce the possibility of misinterpretation by the science nodes.

In steps 2 to 5, switches are closed to connect the converters to the input power cable unless a fault is detected. Low negative voltage and presence of the 3 kΩ resistor insure that switches S1_A or S1_B are not damaged even if a short circuit exists.

In steps 9 or 10, switch S1_A or S1_B may be opened at high voltage. This is an allowed operation because the converter is started at no load; therefore, the current flowing through the switches is almost zero.

After the above operations are completed, any fault at the input of the converters is isolated during the low voltage period; if one converter fails to start, it is isolated and the other converter is started. If a converter fails during normal operation, the startup operations are repeated to start the other converter.

Startup logic circuits have been developed to carry out these operations. The low voltage power supply to power the logic circuits and to start the converters is presented in [7]. The remainder of this paper is focused on the circuit that carries out these logic operations.

III. Logic Circuit for Startup Operations

For convenience, the startup operations in steps 1 to 5 are referred to as switching logic and operations in steps 6 to 11 as A/B selection logic.

A. Switching logic circuit

The purpose of the switching logic circuit is to isolate or connect the power cable coming into the science node to the converters, and check if any fault exists at the converters' input connections (right after switches S1_A and S1_B in Fig. 4). If a fault exists, the related converter is isolated from the input cable. The logic includes different operations at +500 V and -500 V. The functional block diagram of the switching logic circuit is shown in Fig. 5.

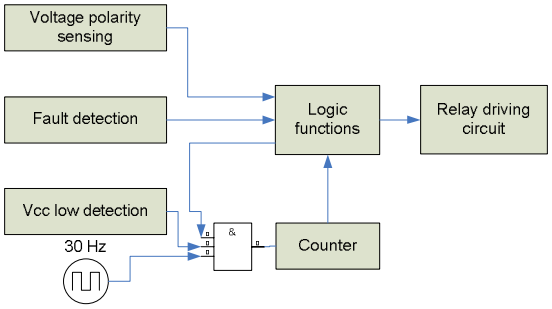

Figure 5. Switching logic circuit block diagram

The purpose of the voltage polarity sensing circuit is to identify the system voltage polarity, and then to determine which operations need to be performed. It compares the potential of sea ground with respect to the startup power supply voltage, using the fact that when the science node input voltage is positive, the startup power supply positive terminal is about 12 V higher than sea ground, and when the science node input voltage is negative, the positive terminal is at about the same potential with sea ground [7].

The operation at positive voltage is relatively simple: opening all switches including S1_A, S1_B and S2. On the other hand, at negative voltage, a series of operations must be carried out in the sequence illustrated in Fig. 6.

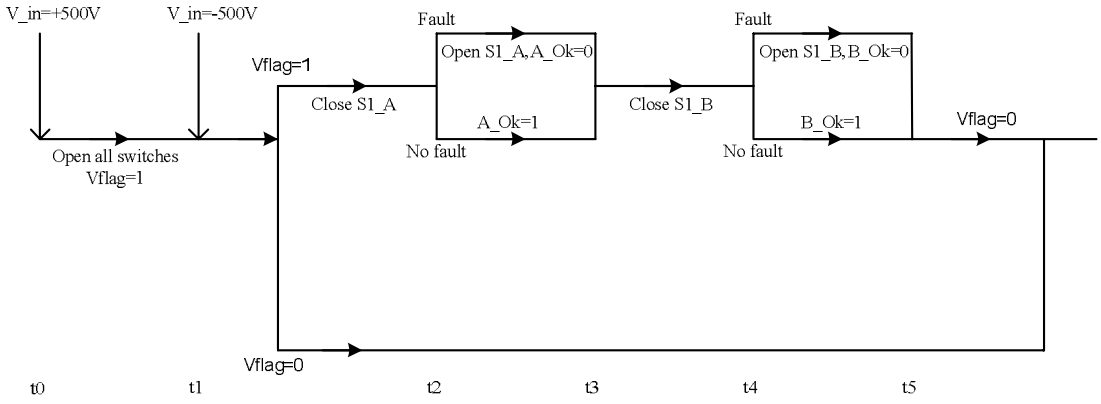

Figure 6. Logic sequence for switching operations

In the diagram shown in Fig. 6, the series of operations are implemented using a clock signal, a counter and appropriate logic gates. In every clock cycle, the counter output moves forward one bit, and the logic functions connected to the next counter output are activated and performed. The method is illustrated in Fig. 7. The operations under negative voltage are carried out from time step t1 through t5.

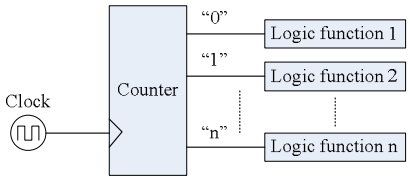

Figure 7. Logic sequence implementation block diagram

In Fig. 6, Vflag is an internal status memory indicating whether or not the operations defined at -500 V have been completed. A_OK and B_OK are two memories indicating the "health condition" of converter A and converter B, respectively. The value and corresponding meaning of the memories are listed in Table 1. The information bits of A_OK and B_OK are sent to the power controllers in the science nodes after the whole system starts up and then transmitted to the shore stations. Thus, the converter connection status is known to the control center. These memories are implemented using small signal latching switches.

Table 1. Register values and meanings of switching logic circuit

state	Vflag	A_OK	B_OK
"0"	Switching operations are finished	Converter A has fault	Converter B has fault
"1"	Switching operations are to be performed	Converter A is OK	Converter B is OK

The task to check for faults at the converters input is challenging because it is required that a current as little as 1 mA should be identified as fault current when the converter is not operating. Ideally, the current sensing should be connected to the high voltage side to better detect any fault. Currently, no accurate current sensing technique is implemented to detect such a small dc current with 10 kV level voltage isolation. A different approach is adopted in the fault current detection circuit, as shown in Fig. 8. The scheme is in fact measuring a voltage signal to get current information. Two voltage dividers are used to measure the voltage across the 3 kΩ current-limiting resister when S1_A or S1_B is closed. If any fault exists at the input of the converters, a current will be flowing through the 3 kΩ resistor. A voltage difference V_d will be detected between the outputs of the two voltage dividers. To reduce the heat dissipation at -10 kV, the voltage dividers have a total resistance of 150 MΩ. The output ratio for the voltage dividers is 1:100, so that it is compatible with the logic circuit input when V_in is at -500 V. However, when the fault current is small, V_d is also very small. For example, if a current of 1 mA is flowing through the 3 kΩ resistor, V_d is only 0.03V. The problem is the well-known problem of measuring the small difference between two large numbers. Further, the large output impedance makes it difficult to measure V_d. The two voltage dividers are carefully selected to closely match each other. High input impedance and common mode rejection ratio are required for the amplifier to detect V_d. An accurate instrumental amplifier followed by carefully designed low pass filter was chosen for completing the task.

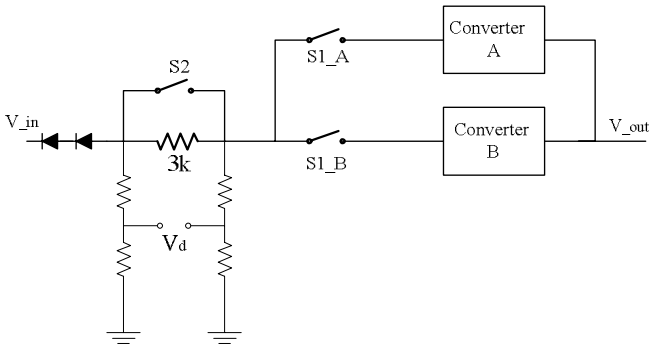

Figure 8. Fault detection method

The Vcc low detection block in Fig. 5 monitors the power supply voltage. The power supply has a very slow pulse-like shape [7, 8], and the logic may not be able to complete its sequence during one burst of power, which

lasts about 200 ms. When the power supply voltage is below a threshold, the logic operations are disabled. Knowledge of the status of the circuit is maintained from one cycle to the next with mechanical switches and by powering the counter with an energy storage capacitor. When the next pulse of power supply comes, the circuit is able to continue carrying out the unfinished logic functions.

The clock signal controls how long each operation in Fig. 6 takes. A short clock period can reduce the energy consumed by the logic circuit, so that less energy is required from the startup power supply. However, there are constraints for the minimum clock period imposed by the operations. For example, closing or opening vacuum switches S1_A or S1_B requires no less than 10 ms. Also, the initial charging current into converters A and B takes 10 to 15 ms to subside. Therefore, the clock period needs to be longer than this time when using the circuit shown in Fig. 8 to detect faults.

B. A/B selection logic circuit

The purpose of the A/B selection logic circuit is to start one of the two converters at an appropriate input cable voltage and switch to the other one if the first one fails. The circuit block diagram is shown in Fig. 9.

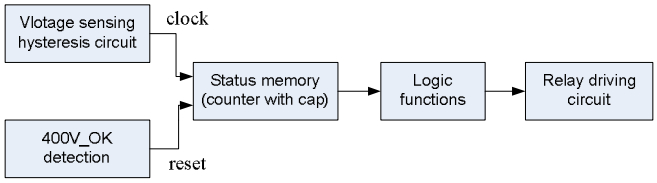

Figure 9. A/B selection logic circuit block diagram

The voltage sensing hysteresis circuit monitors the voltage on the input to the science node. When the voltage is more negative than -5.7 kV, the converter is turned on. When the voltage is less than -5.2 kV, the converter is shut off. The converter operation characteristic is shown in Fig. 10.

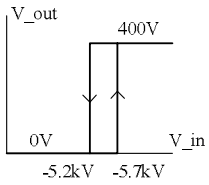

Figure 10. Converter input turn on characteristics

After one converter is turned on successfully, the converter house-keeping power supply (HKPS) takes over to energize the logic circuit, and the supply voltage goes up from 12 V to 16 V. This is shown in Fig. 11. The 400V_OK detection circuit sees this change as a signal indicating a converter has been successfully started.

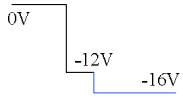

Figure 11. Power supply waveform when a converter is successfully started

Each time the science node power system starts up, converter A is tried first. If converter A does not start, either because a fault is detected and S1_A is opened, or because the converter fails, the logic circuit starts converter B at the next pulse of the startup power supply. The status of the converters is maintained during the interval of two power supply pulses. A counter supported by a large energy storage capacitor is used as a memory for this purpose. The output from the voltage sensing hysteresis circuit acts as the clock signal to trigger the counter.

The logic functions of the A/B selection circuit are described as following.

1) When the input voltage goes more negative than -5.7 kV, a positive pulse from the voltage sensing hysteresis circuit is sent to the counter. Hence the counter output moves forward to "1", and the 10 kV switch S2 is closed to bypass the current limiting resistor. Then the PWM control circuit of converter A will be energized. After converter A outputs 400 V correctly, the counter is reset to "0" by the 400V_OK detection circuit. S1_B is opened to isolate converter B from the input voltage.

2) If for any reason, converter A does not start, the counter stays at "1" waiting for the next power pulse. The next time the startup power supply comes up, the counter receives a clock signal from the voltage sensing hysteresis

circuit. Its output moves forward from "1" to "2", and converter B starts. When converter B outputs 400 V, S1_A is opened to isolated converter A from the input cable.

3) If converter B does not start either, the counter output moves to "3", and S1_B is opened; both converters have failed to start and the science node needs to be repaired.

This process is illustrated in Fig. 12.

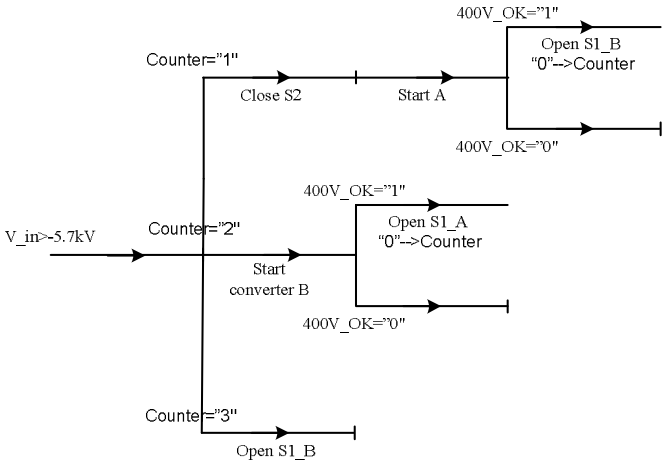

Figure 12. Logic sequence for converter A/B selection

IV. Test Results

A. Switching logic circuit

To test the switching logic circuit, the converter input circuit was simulated using an RC circuit with equivalent values as in the converter input filter. Since the operation at 500 V is rather simple, the emphasis of the test is on the functions at -500 V. Two resistors are connected in front of the circuit simulating converters A and B, and after switches S1_A and S1_B (refer to Fig. 4) to simulate faults. One is 250 kΩ and another is 500 kΩ. Therefore, the fault current is 2 mA and 1 mA at -500 V, respectively. Using the fault sensing circuit shown in Fig. 8, the voltage drop across the 3 kΩ current limiting resistor is detected and shown in channel 2 of Fig. 13. Channel 1 is the counter clock signal (refer to Fig. 5).

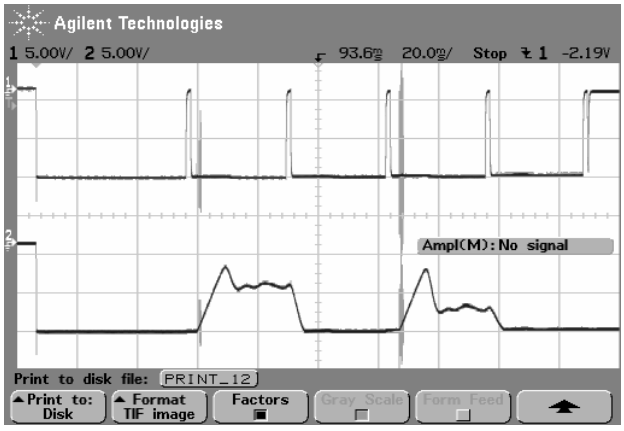

Figure 13. Fault detection circuit waveform when faults exist

Further description of the waveforms shown in Fig. 13 is as following.

1) At the first rising edge of the clock signal, switch S1_A is closed. Thus, the 250 kΩ resistor simulating a fault at converter A is connected to the -500 V input. The voltage across the current limiting resistor is detected as about 6 V.

2) At the second rising edge of the clock signal, S1_A is opened because the fault is detected. Therefore, the current flowing through the 3 kΩ resistor drops to zero. The output of the fault voltage sensing circuit becomes 0 V.

3) At the third rising edge, S1_B is closed. Thus, the 500 kΩ resistor simulating a less serious fault at converter B is connected to the -500 V input. The voltage across the 3 kΩ resistor is detected as about 3 V.

4) At the fourth rising edge, S1_B is opened because the fault is detected. Therefore the output of the fault voltage sensing circuit becomes 0 V for the same reason as in 2).

5) After these operations are completed, the clock signal is disabled to prevent any more switching operations.

When the switch S1_A or S1_B is closed, the converter input capacitance is charged through the 3 kΩ current limiting resistor. This causes the initial spike on the voltage waveform across the resistor, which is not interpreted as a fault by the fault detection circuit.

A waveform without any resistors simulating faults at the converters input is shown in Fig. 14 for comparison. The initial spike on the 3 kΩ resistor voltage waveform is more distinctive in this case, since the current flowing through it goes down to zero after the converter input capacitance is fully charged.

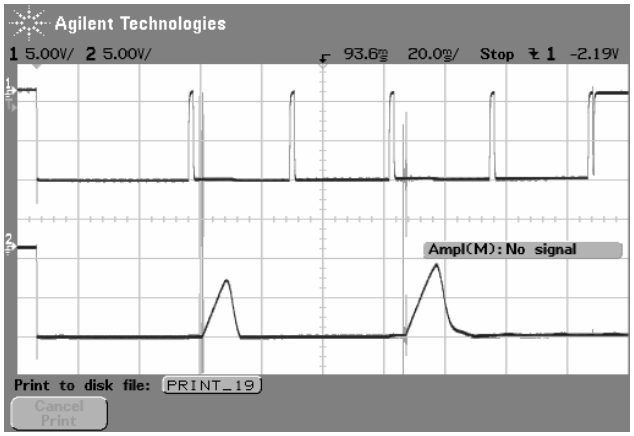

Figure 14. Fault detection circuit waveform when no fault exists

B. A/B selection logic

After a converter starts, the power supply Vcc for the logic circuit is taken over by the converter HKPS. Hence, Vcc goes up from 12 V to 16 V. The waveform is shown in Fig. 15. Channel 1 is the signal to start converter A. Channel 2 is Vcc (Vcc is inverted in the figure). In the test, Vcc is provided by a voltage source simulating the converter HKPS.

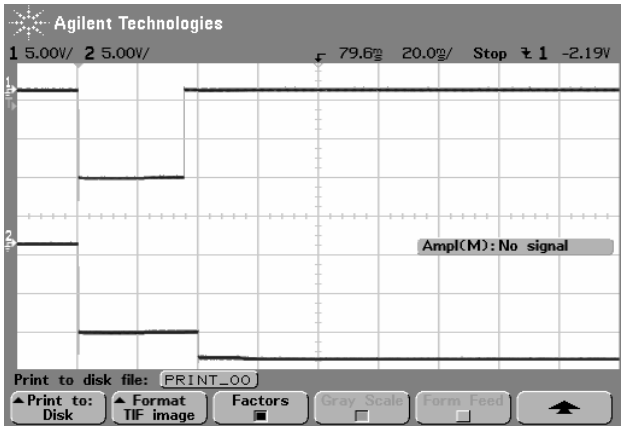

Figure 15. Waveforms of converter start signal and Vcc when converter is successfully started

Fig. 16 shows the waveforms of converter's start signal in Channel 1 and Vcc in Channel 2 when the converter fails to start. Vcc can be seen to drop to 10 V for about 8 ms when trying to start the converter. This is because of the 4 Ω load simulating the converter's MOSFETs driver circuit. Vcc drops to zero after the energy in the startup power supply is depleted.

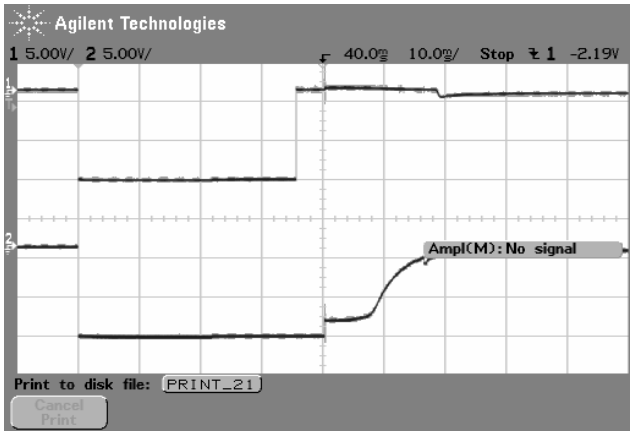

Figure 16. Waveforms of converter start signal and Vcc when converter could not be started

V. Conclusion

The NEPTUNE power system poses challenges in system operations, controls, and hardware design. First, reliability has to be a significant design objective. The importance of a reliable power system is because maintenance can be done only during certain times of the year, and is very costly. Second, the need for the autonomous start-up of one of two 10 kV to 400 V dc-dc converters in the science node on the seafloor makes the design particularly difficult. Before the converter starts, there is no local power and no communications to shore. Yet it is essential to check for faults prior to applying full voltage to the converter, and to maintain knowledge of the converters' status even when power is removed.

In this paper, the startup operations for the science node power system are described. The design aims to impose minimum stress on the components in order to achieve high reliability. Also, the operations enable the system to start autonomously.

The circuit to implement the operations are developed and tested. The results presented here verify the functionality of the system.

Acknowledgments

This development effort is sponsored by the National Science Foundation grant OCE 0116750, "Development of a Power System for Cabled Ocean Observatories."

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